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Low Static Power and High Throughput Wave- Pipelined Global Interconnect Circuits

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Section 1: Introduction

As every successive generation of CMOS transistors continues to shrink, power consumption has become one of the greatest impediments to future developments in the semiconductor industry [1]. As described by Moore's Law, smaller feature sizes allow a higher number of transistors to be housed on a microprocessor or application specific integrated circuit (ASIC), creating more complex computing systems (e.g. multicore processors) that contain a growing number of elements. Because overall power consumption is directly related to the number of transistors and wires in a chip, Moore's Law can have dramatic effects on the power required to operate future microprocessors.

While there are several components to power consumption, the power that is dissipated during quiescent, non-switching circuit periods (known as "static power") is the component directly linked to the number of transistors in a chip. Static power is consumed by every period independent of whether switching is taking place. Quiescent periods can account for nearly 20% of a circuit's operation [2] and these periods occur when leakage power is flowing but transistor switching is not taking place. As technology miniaturizes, other components of power dissipation such as dynamic power per transistor (to be discussed in Section 2) are scaling with the technology size. However the rate of static power dissipation is growing so quickly that it overshadows the lowering rates of dynamic power and leads to an overall growth in power consumption.

Industry is currently investigating techniques to reduce the increasing amount of power lost during quiescent periods. Among those techniques, increasing the threshold voltage of circuit transistors appears to hold promise. The threshold voltage V_t is the voltage required to switch a transistor between a non-conducting and conducting state.

The amount of static power dissipated during circuit operation is inversely related to this voltage such that an increase in V_t will lead to an exponential reduction of power consumption (the causes of this dependence will be investigated in Section 2).

An unfortunate side effect of increasing V_t however, is that the operating speed of CMOS circuits will be reduced. If a chip designer decides to increase the threshold voltage to reduce the standby power consumption of his devices, he will have to tolerate a lower operating frequency and a “slower” commercial product. For on-chip communication, however, a technique known as “wave-pipelining” can be implemented across global interconnect circuits to combat the loss in throughput because of V_t scaling. Global interconnects are large, cross-chip wires that transport data over relatively long distances and typically take considerable amounts of time. Wave-pipelining breaks up the trip across these wires into multiple stages, so that more than one signal can be on a wire at any given time. So in the amount of time typically required to send one signal across a line, several signals can now be sent, increasing the number of bits per second (i.e. throughput) transmitted across the interconnect. This single channel serial implementation does not require any synchronization overhead or mechanisms.

This research project will explore a low-power, high-throughput design using high threshold voltage transistors in combination with wave-pipelining techniques across global interconnect circuits. Reducing the static power consumption of integrated circuits will lead to more power efficient devices. Through the use of wave-pipelining, an increase in throughput will create faster, higher frequency operating circuits.

The theories presented in section 4 will be verified using HSPICE circuit simulations of past and future transistor technologies ranging from transistor gate sizes of 130nm to 32nm. These technology nodes represent the estimated shrinking transistor sizes from 2001 (130nm) to 5 years into the future (32nm) [3]. This thesis will outline a theory developed to produce a low-power, high throughput design, the work performed to verify this theory, and the results that were gathered. Section 2 will give background information on the semiconductor physics involved in this project and will also describe the cause-and-effect relationships needed to justify the statements given in the Introduction. Section 3 considers current work in this area and outlines experiments that have already been performed. Section 4 will define the methods to be used in performing this research. The final section will provide the simulation results, draw formal conclusions from the performed research, and suggest future research directions.

Section 2: Background

The Introduction section leaves several important questions unanswered:

- 1. What are the types of power consumption?*
- 2. What factors cause static power consumption?*
- 3. Why is power consumption increasing as technology gets smaller?*
- 4. Why will an increase in V_t reduce static power consumption and throughput?*
- 5. What is wave-pipelining and how will it help?*

The first three questions will be answered in Sections 2.1, 2.2, and 2.3; which will provide basic background information on the causes and types of power consumption (i.e. define the problem). Questions three and four will be answered in Sections 2.4 and 2.5; which will give a detailed explanation of the proposed research (i.e. solve the problem).

2.1 Types of Power Dissipation

Power dissipation is traditionally divided into two types: dynamic and static power. While dynamic power is consumed during the switching periods that superthreshold current runs through a transistor, static power is lost during quiescent periods, when subthreshold current runs through a transistor. For a better understanding of the distinction between these two types of power dissipation, we first consider the operation of a transistor.

In order for a transistor to conduct current, a certain amount of charge must be present in the transistor's "conducting layer" that is stored in a gate capacitor. When the transistor's gate capacitor is charging up, a current I_{line} is running across a line connected to the gate with a resistance R_{line} . Power is dissipated in the form of heat whenever the

current moves across the line according to the equation $P = (I_{\text{line}})^2 R_{\text{line}}$ [4]. The power lost during the charging and discharging of the transistor's gate is known as *dynamic power*.

However a circuit's transistors are not continually switching off and on. During certain inactive (quiescent) periods, the transistors' state will remain constant and there is no superthreshold current being used to charge or discharge the output node of a logic gate. With no superthreshold current flowing through the transistor, there is no dynamic power being dissipated; however there may still be a small subthreshold current, I_{leakage} , flowing through the device. This is known as a "leakage" current because it is an undesired effect, analogous to a wooden barrel leaking water. This current leads to a dissipation of *static power* according to the formula $P = (V_{\text{dd}} I_{\text{leakage}})$, where V_{dd} is the supply voltage for the digital circuit.

2.2 Causes of Static Power

There are three components that lead to the leakage current described in Section 2.1. These components are labeled below in Figure 2.2.1, which shows a cut-away view of a p-channel MOSFET transistor. Taken together, these currents make up the overall leakage current such that $I_{\text{leakage}} = I_{\text{bulk}} + I_{\text{channel}} + I_{\text{gate}}$.

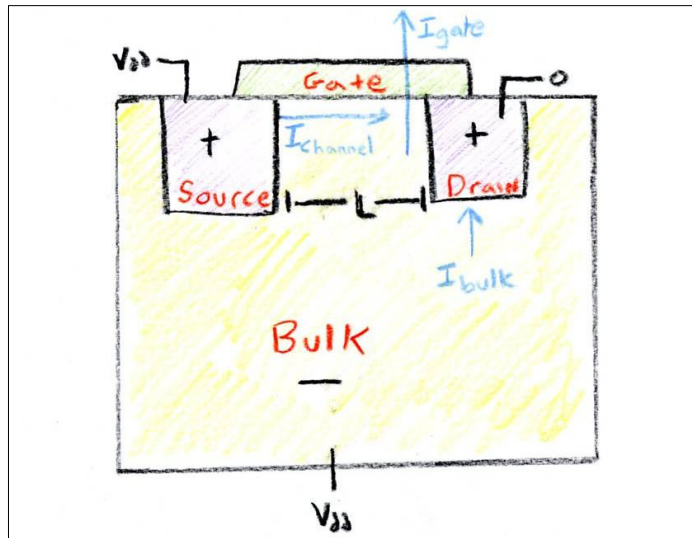


Figure 2.2.1: Cut-away view of a p-type transistor

The bulk leakage current (I_{bulk}) is formed at the reverse biased PN junction interface (for the p-type transistor shown above, this interface is between the drain junction and the bulk). This reverse bias causes a small minority carrier current to flow. This current flows from the bulk through the drain and is subject to the resistance found in both regions (the power is dissipated due to this resistance as discussed above).

The gate leakage current (I_{gate}) flows across the gate capacitor region out of the transistor. When the transistor is conducting current, a conducting channel exists below the gate between the source and drain. Due to the thinness of the gate, a very small amount of current carriers can quantum mechanically tunnel through the gate oxide (which is designed to act as an insulator) and out of the device.

The final type of leakage current (I_{channel}) flows from the source to the drain when no conducting channel is present. This is the dominant source of leakage current in modern transistors and is directly dependent on the length L of the gate (i.e. the distance between source and drain). With a smaller length L , the distance required for current to jump from a positive source region across a highly resistive negative region (bulk), to a grounded

region (drain) is smaller. With a smaller distance, there is more source/drain electrostatic interaction, that causes a drain induced barrier lowering (DIBL). This gives a higher probability of current carriers making it across the channel, thereby creating larger leakage current.

The reason for this can best be explained by using an energy band diagram of the source – gate – drain region of the transistor. These diagrams illustrate the energy barriers that carriers must reach for current to flow. Figure 2.2.2 shows the energy band diagram of a typical n-channel MOSFET transistor. In order for current to flow across this transistor, the current carriers (represented as black dots in the source) must have enough energy to surpass the gate barrier (represented by a red line). Since the number of carriers existing at each energy level drops off exponentially, only a small number of carriers will have enough energy to cross that gate region, and there will be a very small current.

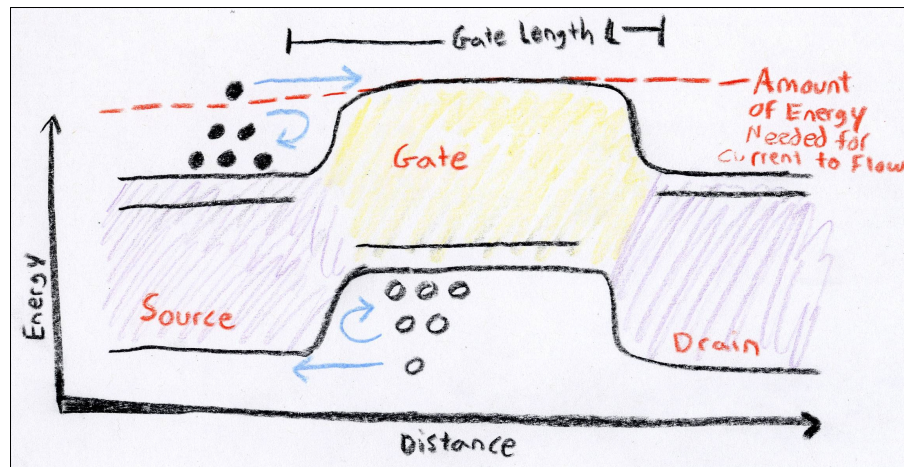


Figure 2.2.2: Energy band diagram of an n-type transistor

If we reduce the gate length L , the source and drain regions begin interacting with one-another. Figure 2.2.3 shows the energy band diagram with a very small gate length. Because the two sloped regions are now crossing at a lower level than in Figure 2.2.2,

there is a smaller energy requirement for current to flow. With a smaller energy barrier, more carriers are able to overcome this barrier and contribute to the leakage current.

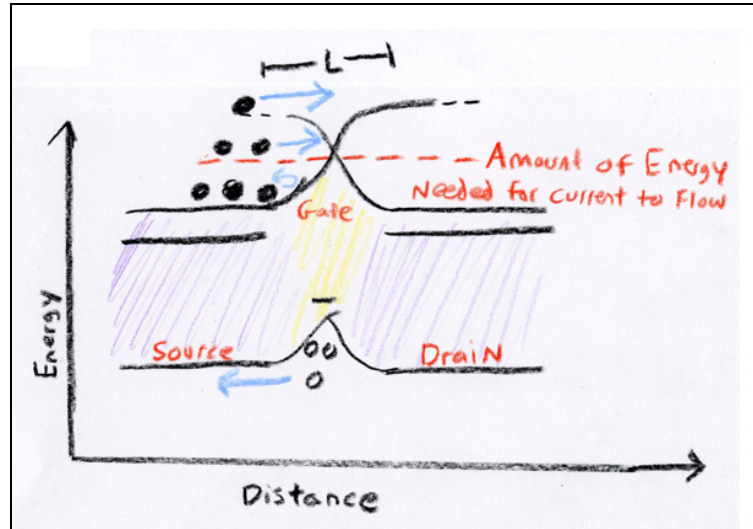


Figure 2.2.3: Energy band diagram of an n-type transistor with small L

2.3 Smaller Technology Leads to an Increase in Static Power

As the minimum feature size shrinks, the dynamic power dissipation per transistor shrinks, due to a smaller amount of current needed to charge up the transistor gate capacitor [5]. However the rate of static power dissipation per transistor has actually increased. The primary reason for this increase is an increase in the channel leakage current I_{channel} . As discussed in Section 2.2, with a smaller gate length L this current will become larger due to DIBL. The gate lengths that were tested in this research range from 130nm to 32nm and represent a growing rate of leakage current with progressively smaller gate sizes. With larger leakage current, more static power will be dissipated according to $P = V_{\text{dd}} I_{\text{leakage}}$.

2.4 Effects of Increasing the Threshold Voltage

Additional doping will increase the number of majority carriers in the substrate, thereby increasing the threshold voltage V_t . This voltage is formally defined as the gate voltage at which the concentration of minority carriers in the inversion channel are equal to the concentration of majority carriers in the bulk. By increasing the substrate doping, there is a higher concentration of majority carriers and a higher gate voltage (V_t) will be required to reach inversion. Therefore higher doping can be used to increase the threshold voltage. A higher substrate doping will have several effects on the operation of the transistor.

The most beneficial effect of increasing the threshold voltage is a reduction of leakage current (and thus static power). An energy band diagram can be consulted to understand why the leakage current is reduced.

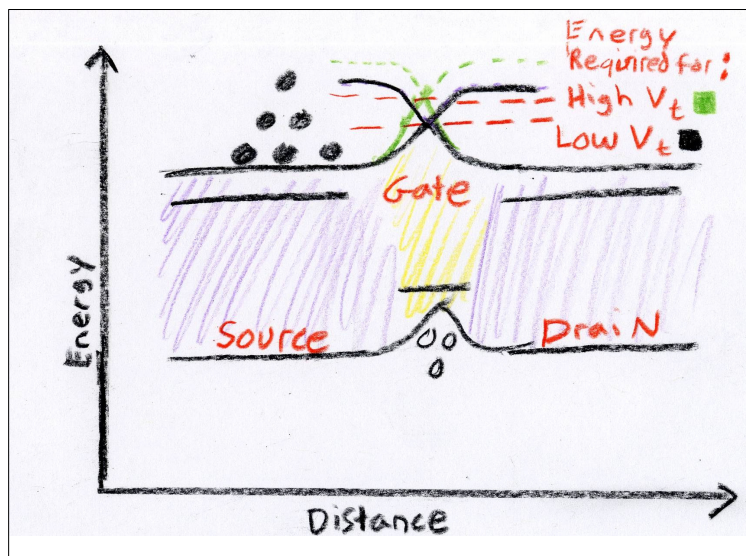


Figure 2.4.1: Energy band diagram with small L and higher doping

Figure 2.4.1 is an exact copy of Figure 2.2.2, with one exception: the green lines represent the energy barrier required with a higher substrate doping (an increased V_t).

The difference in levels between the source and gate is directly related to the amount of

doping in each region. If we increase the channel doping, the depletion regions of the source and drain junctions become smaller in the channel and reduce their interaction. In addition, the higher doping increases the built-in potential for the source drain junctions, and as seen in Figure 2.4.1 has a tendency to increase the barrier height in the channel. Subsequently fewer carriers will be able to overcome this barrier and contribute to the leakage current, which results in less static power dissipation.

A secondary, less-desired effect of increasing the threshold voltage is a reduction in circuit performance. A major element of performance is how long it takes each gate capacitor to charge and discharge or switch from non-conducting to conducting (and vice-versa). This element contributes to the maximum switching frequency or throughput of the CMOS circuit. This switching frequency can continue increasing until it reaches a level at which there is just enough time for the gate capacitor to fully charge. If the frequency is increased above this level, there will not be enough time for the gate capacitor to charge or discharge and the circuit's transistors cannot correctly transition between conducting and non-conducting.

The amount of time it takes for the gate capacitor to charge depends on the amount of drive current being fed into the capacitor (I_{drive}). With an increased threshold voltage, there will be a smaller amount of drive current charging the gate capacitor, and it will take longer for the gate to switch between conducting and non conducting (effectively reducing the number of signals per second or throughput). The reason I_{drive} will be reduced is illustrated in Figure 2.4.2, which plots the voltage of the gate versus time.

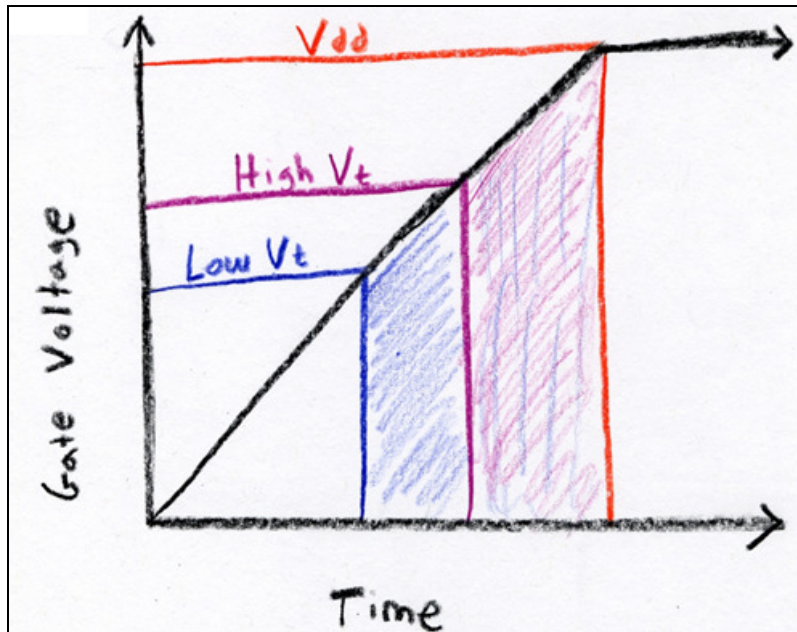


Figure 2.4.2: Plot of Gate voltage vs. Time

As the gate begins charging, there is effectively no drive current (leakage current will be ignored) because it is in the subthreshold regime. After reaching the threshold voltage, a small current begins to flow and continues to grow until the gate is fully charged to V_{dd} . This current will be used to drive the next transistor in the circuit and is equivalent to I_{drive} for that gate. As shown in Figure 2.4.2, with a low V_t (shown in blue), there will be more voltage between the threshold voltage and V_{dd} , so a stronger drive current will be formed than with a high V_t (shown in pink). In addition, the larger V_t has a tendency to decrease the conductivity of the channel due to less minority carriers in the channel for a given gate voltage. This results in a smaller drive current for the transistor with a higher threshold voltage.

Therefore an increased threshold voltage will have two effects on the operation of a circuit: the amount of static power dissipation will be less due to an increased energy barrier and less leakage current, and the throughput will be reduced due to a smaller drive current.

2.5 Wave-Pipelining

Global interconnect circuits contain large, across chip wires that account for a major delay (or latency) when sending a signal from one end to the other. When signals are sent across long wires, the amount of current that enters the wire will be substantially greater than the amount of current that exits the wire due to the parasitic resistance of the wire. Global interconnects will be used to drive a gate capacitor at the end of its line, so with a smaller drive current it will take longer to charge the gate and substantially decrease the circuit's throughput. This problem can be fixed using wave-pipelining.

To explain the principles behind pipelining, an analogy may be drawn to washing a batch of laundry. When washing clothes, a resident can move one load of laundry from the washer to the dryer to the closet and then begin the next load, or the resident can break the process into multiple stages, adding a second load of laundry to the washer as the first begins the drying cycle. It is clearly more efficient to complete multiple tasks at the same time than to take each batch of laundry from start to finish before beginning the next. While it will take the same amount of time to complete the first load, every subsequent load will be completed in a fraction of the time.

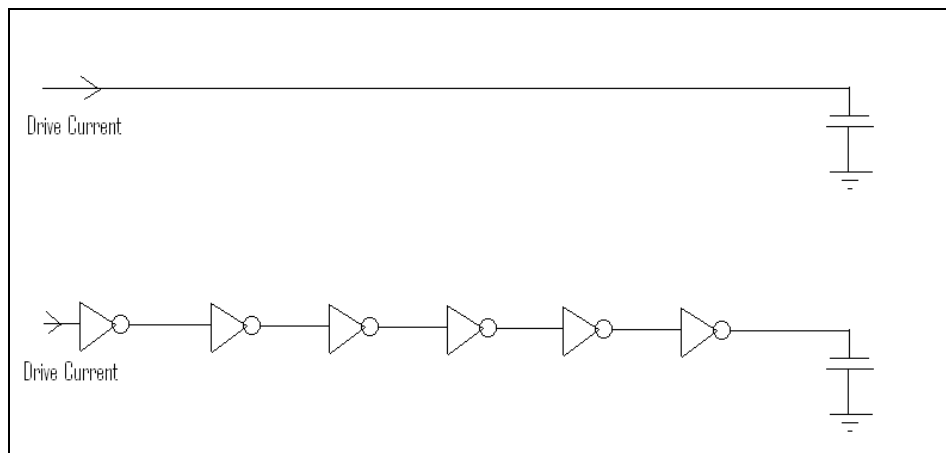


Figure 2.5.1: Standard and Pipelined interconnects

The laundry analogy can be applied to the operation of global interconnect circuits. The top part of Figure 2.5.1 shows a standard interconnect and gate capacitor, while the bottom half of this figure is a pipelined implementation. Using wave-pipelining, repeaters are inserted into the interconnect that periodically boost the drive current across the wire because the resistance per segment is reduced with shorter wire segments. With a much stronger drive current, the wave-pipelined gate will charge faster and have a higher throughput than its traditional counterpart. The insertion of repeaters will also allow for multiple signals to be sent along the interconnect at any given time, similar to the laundry analogy presented earlier.

The insertion of repeaters will minimize the parasitic effects of an interconnect wire. However as the number of inserted repeaters grows, the improvement in throughput will eventually saturate with continued repeater insertion. This is due to the charge-up time of the gate capacitor in each repeater. While the parasitic effects of the wire initially dominate the throughput, as the number of repeaters grows, the parasitic effects are dominated by the transistor characteristics (the gate capacitor).

Section 3: Current Work

Over the last 60 years, the microelectronics industry has continuously reduced the size of features on a micro-chip according to Moore's Law, a theory that predicts the number of elements on a standard chip will double every 12 to 18 months [6]. The International Technology Roadmap for Semiconductors (ITRS) is a global organization responsible for projecting future operation of semiconductor electronics. As the smallest transistor features begin to approach 22nm in length, ITRS has detailed impending power dissipation rates for static and dynamic energy. Among their conclusions, this organization projects that static power will become the largest contributor to power consumption by percentage at the 22nm level [1]. Under these assumptions, Intel Chairman Andrew Grove has labeled static power dissipation as a limiting factor in the future development of microprocessors [7]. Other researchers have labeled its reduction as imperative in the design of future circuits [8].

3.1 Reducing the Amount of Static Power Dissipated

With miniaturization as a clear priority in the future development of semiconductors, engineers have begun investigating techniques to suppress quiescent (static) power dissipation. Due to the inverse dependence between this dissipation and the threshold voltage V_t (or the amount of power necessary to switch a transistor between conducting and non-conducting), many have suggested [9,10] incorporating high- V_t transistors is the optimal technique for reducing energy dissipation.

Research performed in [11], for example, used a dual-threshold voltage technique to find an overall power reduction of up to 29.45%. The methods presented use low threshold transistors for elements in the critical path, which is the path through the circuit

that requires the most time to complete, and high threshold transistors for gates off the critical path. This reduces the static power consumption that takes place on the non-critical path gates while minimizing the impact on overall system performance.

However an increase in the threshold voltage will cause an increase in the amount of time required to “switch” a transistor between the on and off states, effectively reducing the performance of a circuit. This is due to the interdependency of the circuit’s operating frequency and threshold voltage. Two notable techniques have been proposed to increase the speed of a circuit, and these are examined in sections 3.2 and 3.3.

3.2 Using Repeater Insertion to Increase Throughput

The first concept stems from work conducted by Deodhar in [12] who investigates the insertion of buffered ‘repeaters’ in future global interconnect circuits to create a wave-pipelined approach to increasing the throughput. This work focuses primarily on decreasing dynamic power dissipation; however the proposed technique could easily be transformed to increase throughput in circuits that employ static dissipation reduction methods. Deodhar's work explores the effects of reducing a circuit's supply voltage, the highest operating voltage of the circuit. With dynamic power as a function of the square of the supply voltage, a reduction in this variable will lead to considerable reductions in dynamic power [12]. However as a consequence of lower supply voltages, transistors will experience smaller drive current thereby reducing transistor performance (particularly throughput).

The authors in [12] propose to compensate for this loss in performance through the use of periodic repeater insertion in the global interconnects. This would create a 'wave-pipelined' design whereby multiple signals may exist on a given line at the same time. In

addition, the authors in [12] develop an optimization between the supply voltage and number of repeaters (or stages) to generate minimum dynamic power loss with maximum throughput.

3.3 Using a Dual Supply Voltage to Increase Throughput

The second technique for increasing circuit speed is based on a ‘dual supply voltage’ design, suggested by M. Khellah to reduce power loss while maintaining adequate throughput performance [13]. This technique operates by supplying circuits with a high supply voltage during transition periods to increase speed (the circuit throughput is proportional to V_{dd} [5]). The supply voltage is lowered during quiescent periods so that power is not wasted. Power improvements under this method will occur mostly in dynamic consumption (dynamic power loss is proportional to V_{dd} [5]). Performance improvements were measured by [14] and are shown in Table 1. Under these measurements, this technique causes a 22% reduction in static power dissipation, as well as a 24% reduction in dynamic power loss. Circuit delay (a measurement of speed) was reduced by 3%.

Table 1: Improvements reported by [8] through the use of dual- V_{dd}

Bus Design Technique	Dynamic Power	Static Power	Delay	Dynamic/Static Power Ratio
Traditional Design	1.00	1.00	1.00	11.1 / 1
Dual - V_{dd}	0.76	0.78	0.97	10.9 / 1

3.4 Lessons Learned

While work has been performed in both reducing static power dissipation (through the increase in V_t) and increasing throughput (through repeater insertion and a dual- V_{dd} design), there has been no conclusive research on applying both methods. This project will apply both of these existing techniques to optimize circuit performance.

Section 4: Methods

This project demonstrates that a low power, high throughput global interconnect circuit can be constructed through the use of high threshold voltages and wave-pipelining. In order to verify the theory presented in this thesis, HSPICE simulations were performed on global interconnect circuits and the static power, total power, and throughput measured. Results were taken in the following order:

1. Static power simulations were run on a basic global interconnect circuit with varying technology sizes. The sizes ran from 130nm to 32nm and the simulations verified that the percentage of static power dissipation is increasing with decreasing technology.
2. For each technology size, both high- V_t and low- V_t global interconnect circuits were constructed and static power simulations run on each. It was demonstrated that the circuits with a higher threshold voltage have a lower levels of static power dissipation.
3. Using the high- V_t repeaters, throughput was measured on each global interconnect with a varying number of repeaters inserted. For each global interconnect circuit, the maximum operating frequency was recorded. A plot was be generated for each technology size of # of repeaters vs. throughput. Since the operating frequency as a dramatic effect on the amount of total power dissipated (and thus the percentage of static power), simulations were re-run on each circuit using the determined frequency so that an accurate percentage of static power was be recorded.

The transistor models used in this research are the Berkeley Predictive Technology Models (BPTM) found at <http://www.nanohub.com>.

4.1 Measuring Static Power

Static power will be measured in the basic inverter circuit shown in Figure 4.1.1 below. Using HSPICE software, we can determine the average amount of leakage current of the inverter in each of its possible states. If we also know the transistor's size, the amount of static power dissipated is simply $P = (V_{dd} I_{leakage})$. Since this rate is independent of the transistor's location in a circuit, the static power dissipation calculated from an inverter can be multiplied by the number of invertors in any circuit to determine the amount of static power dissipated in that circuit. A constant voltage will be given as an input to the circuit and measurements will be taken for both a low level input (shown on the left hand side) and high level input (shown on the right).

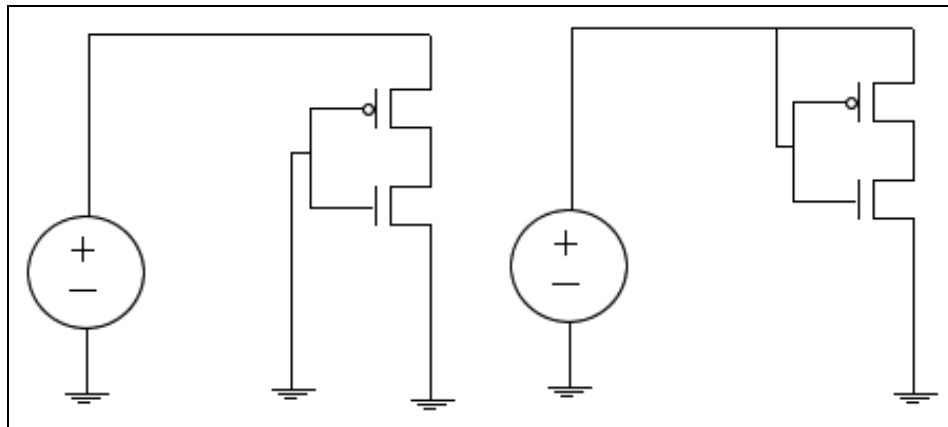


Figure 4.1.1: CMOS inverter circuit used for Static Power extraction

Once the amount of power dissipated is known, the amount of energy lost can be calculated using the equation $E = 2T * P$; where E is the amount of energy, T is the period of the global interconnect circuit, and the factor 2 accounts for both the rise and fall time of the circuit. This equation is derived from the fact that power is energy

dissipated per unit time, and the time over which static energy is dissipated in a global interconnect circuit is the period of the input wave.

4.2 Measuring Total Power

In order to determine the percentage of static power dissipated, it is necessary to calculate the total power lost in each global interconnect circuit.

4.2.1 Circuit Model

Figure 4.2.1.1 shows the circuit model that was used for global interconnects. The input waveform V_{in} is the signal that was propagated across the global interconnect, and determined the maximum operating frequency of the circuit. A supply voltage V_{dd} was attached to the source of each PMOS, and ground was attached to the source of each NMOS. The line began with a repeater segment followed by 5 RLC segments, which was used between each repeater to simulate a wire. This pattern continued for N repeater segments until the end of the wire was reached. Simulations were run for $N = 1, 5$, and 10 repeater segments.

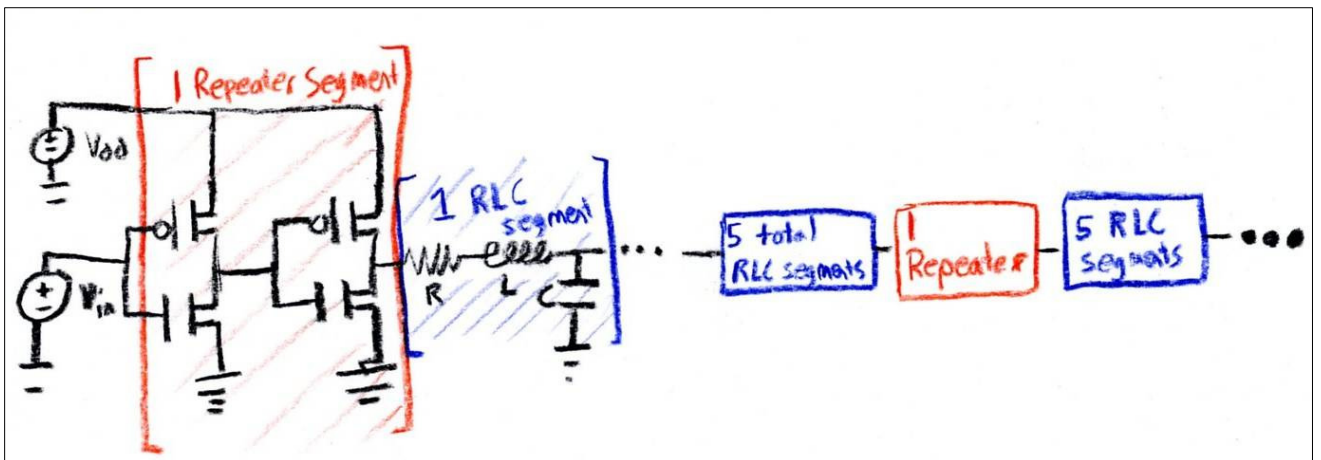


Figure 4.2.1.1: Global interconnect circuit model

4.2.2 Procedure

The V_{dd} voltage source provides a reference for HSPICE to measure the total amount of energy flowing into the circuit. HSPICE can calculate the amount of current flowing out of the source terminal, and the total amount of energy can be calculated using the formula: $E_{tot} = V_{dd} \int I_{Vdd}(t) dt$.

4.3 Measuring Throughput

Throughput measurements will be taken using HSPICE software. Simulations will be run on the same circuits as in Section 4.2.

4.3.1 Interconnect Model

Since the circuit's throughput is directly governed by the parasitic effects of the global interconnects, it is critical that accurate models be used during simulation. Each interconnect will be modelled using a distributed RLC network as shown in Figure 4.3.1.1. These networks will mimic the effects of a long wire and the higher the number of RLC segments used, the more accurate the model will become.

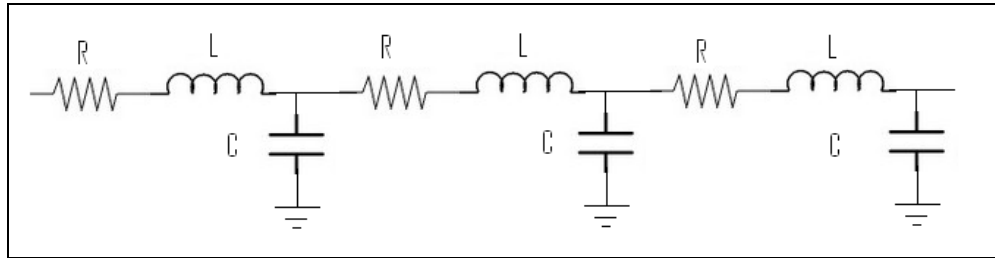


Figure 4.3.1.1: RLC model for interconnects

The simulations in this research will use 5 RLC segments for each interconnect. The **inductance** parameter L will be set to 0 due to the negligible amount of inductance in these wires. The **capacitance** will be determined using the Raphael Interconnect Library [15]. This model will assume capacitance contributions from two adjacent wires and metal above and below the wire, as shown in Figure 4.3.1.2.

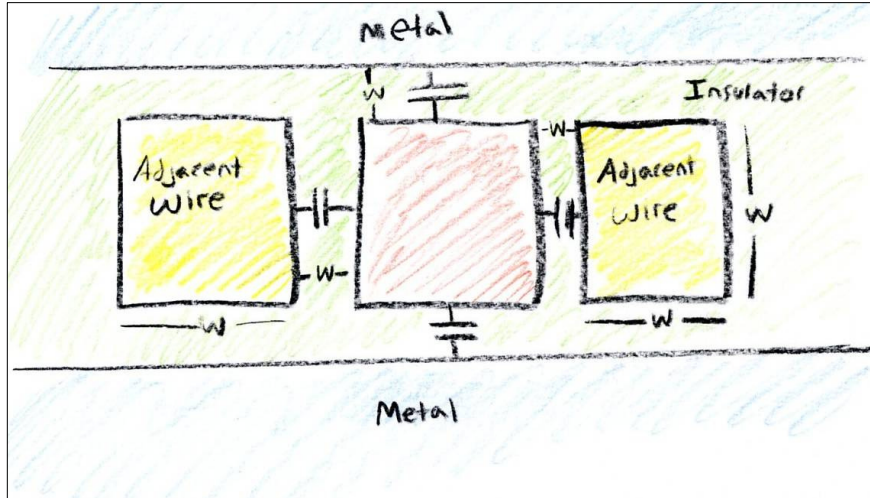


Figure 4.3.1.2: Wire capacitance model

The middle square represents the wire being modeled. The wire is assumed to be square with dimensions equal to W , the minimum global interconnect width as defined by the International Technology Roadmap for Semiconductors [1]. Values for the insulator permittivity (ϵ_v) of each technology generation were taken from this source and used to compute the capacitance. All separation spaces around the wire are equal to the minimum width W .

The **resistance** per unit length R is equal to the resistivity of copper ($\rho = 2.2 \times 10^{-6} \Omega \text{ cm}$) divided by the cross sectional area of the wire ($R = \rho / (W^2)$). The values for the minimum global interconnect width have been taken from the ITRS 2002 edition, and are listed in Table 4.3.1 along with the corresponding resistance, inductance, and capacitance that was used in this research. An interconnect length of 5 mm was also used.

Table 4.3.1: ITRS Parameters

Technology Size	Wire Dimension	ϵ_v	Inductance	Capacitance	Resistance
130nm	335 nm	3.6	0 H/cm	$2.00\text{e-}12 \text{ F/cm}$	$1,960 \Omega/\text{cm}$
90nm	230 nm	3.1	0 H/cm	$1.73\text{e-}12 \text{ F/cm}$	$4,159 \Omega/\text{cm}$
65nm	145 nm	2.7	0 H/cm	$1.50\text{e-}12 \text{ F/cm}$	$10,464 \Omega/\text{cm}$
45nm	102.5 nm	2.1	0 H/cm	$1.17\text{e-}12 \text{ F/cm}$	$20,940 \Omega/\text{cm}$
32nm	70 nm	1.9	0 H/cm	$1.06\text{e-}10 \text{ F/cm}$	$44,898 \Omega/\text{cm}$

4.3.2 Procedure

Throughput was measured on high threshold voltage global interconnect circuits. Simulations were run for a varying number of repeaters on each technology size to determine the optimal number of repeaters with respect to throughput.

The maximum operating frequency of each circuit was determined by measuring the output voltage waveform with respect to time. The interconnect's input wave was set with an initial baseline frequency. This frequency was increased until the interconnect's output voltage just reached 90% of the supply voltage and the maximum operating frequency was determined [12]. If the input frequency is increased past the maximum operating frequency, the transistor gate capacitors will not have enough time to charge up before switching signals and the circuit will not operate correctly.

Section 5: Results

HSPICE simulations on a set of global interconnect circuits yielded results that correlate to theory presented in this thesis, namely:

1. The miniaturization of microelectronic circuits lead to an increased rate of static power dissipation. (**Section 5.1**)
2. An increase in the threshold voltage of the transistors in these circuits reduced the rate of static power consumption. However increasing this voltage also reduced the throughput of the circuit. (**Section 5.2**)
3. Implementing a wave-pipelining technique through the use of repeater insertion ameliorated the loss in throughput caused by the increase in threshold voltage. (**Section 5.3**)

Verification of these statements shall be performed using the methods described in Section 4, above.

5.1 Effects of Miniaturizing Technology

Power dissipation measurements were taken using HSPICE software for various technology nodes with the high performance low- V_t process and the results are listed in Table 5.1.1. The static power as a percentage of total power was also calculated and appears in this table. To calculate the static energy and average power dissipation, it is assumed in Table 5.1.1 that there are two transitions (i.e. low-to-high and high-to-low) over an interval of 10ns. These simulations were performed on a basic repeater element (two inverters). In order to perform the simulations at different technology nodes, the gate widths and supply voltage were scaled down by the same factor as the gate length in accordance with the ITRS.

Table 5.1.1: Static vs. Total Power as Technology Miniturizes

Technology	Static Power (nW)	Total Energy (J)	% Static Power
130	1005.54	4.72E-13	4.086
90	1324.64	2.42E-13	10.422
65	1857.38	1.53E-13	21.968
45	2894.80	1.14E-13	46.766
32	3503.00	7.09E-14	93.864

As seen in Figure 5.1.1, the percentage of power that is static power increases exponentially. These results demonstrate that as circuit technology continues to progress (get smaller), static power is becoming a larger percentage of the total power consumption. If left unchecked, it will dominate overall power consumption as transistor gates shrink below 65nm in length. This data justifies the need for low-power considerations in future designs.

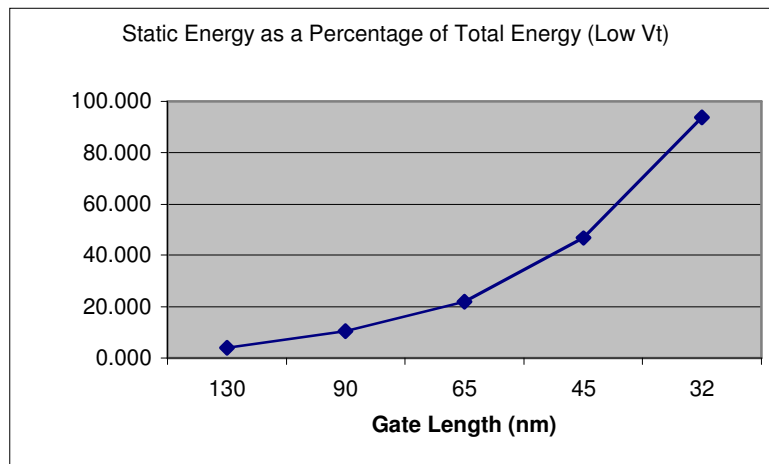


Figure 5.1.1: Static Energy Percentage vs. Gate Length with two binary transitions over a 10ns interval

5.2 Effects of an Increased Threshold Voltage

The basic repeater element was reused to perform a comparison between high and low threshold voltage circuits. The low threshold voltage was defined as 15% of the supply voltage, while the high threshold voltage was 30%. Using these percentages, two sets of library files were downloaded from the Berkeley Predictive Technology Model

website (<http://www.nanohub.com>) for every technology size tested in Section 5.1. Both static and total power simulations were run on the repeater circuit for high and low threshold voltages, and the results are plotted in Figure 5.2.1. The same assumptions as stated in Table 5.1.1 apply (e.g. two transitions over a fixed time interval of 10ns).

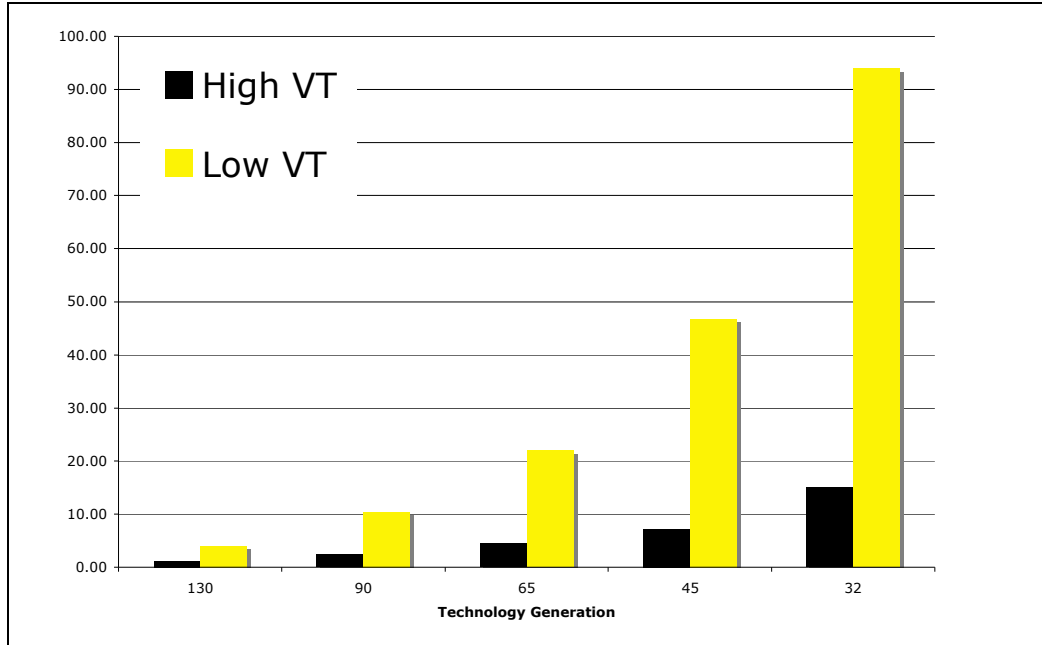


Figure 5.2.1: Static Energy Percentage vs. Gate Length for both High and Low V_t

This graph clearly indicates that high threshold voltage devices offer a more power efficient solution. While differences in static power consumption are minimal at the 130nm generation, as gates approach 32nm in length the static power of a low V_t device is almost 6 times as much (93% vs. 15%). Because a switching period of 10ns was used to calculate the average power consumption, the numbers in Figure 5.2.1 will vary depending on changes in this temporal activity.

5.3 Effects of Wave-Pipelining

A wave-pipelined circuit was then constructed using repeaters and RLC elements as described in Section 4.3 above. This circuit employed high V_t transistors. An input waveform was chosen with an arbitrary pulse width. This pulse width was then varied so that the output waveform just reached 90% of V_{dd} . This final pulse width was assumed to be related to the maximum operating frequency of the global interconnect channel.

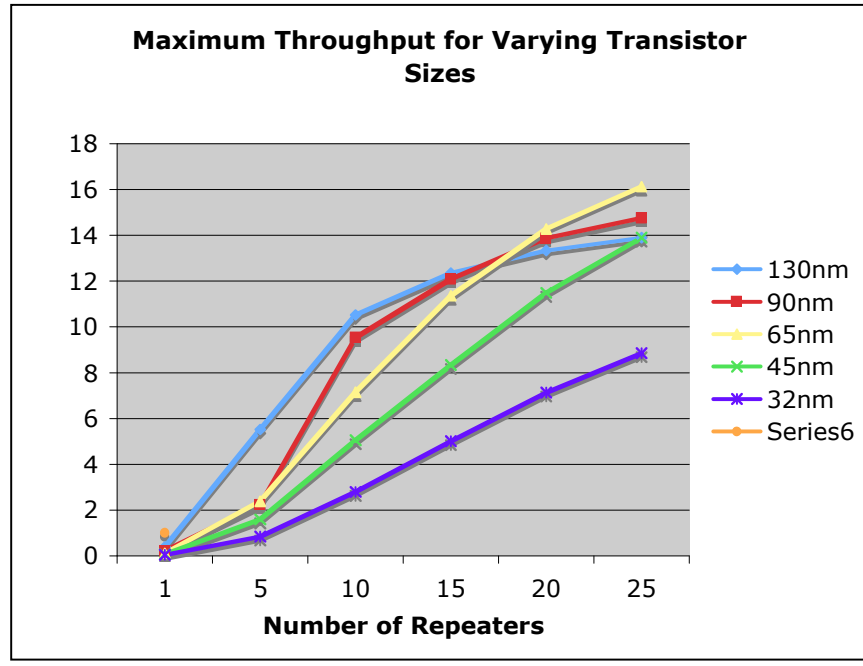


Figure 5.3.1: As the number of repeaters increases, so does the throughput.

As shown in Figure 5.3.1, the maximum throughput increases as more repeaters are inserted into the circuit. Each color in this figure corresponds to a different technology node. Simulations were run from 1 to 25 repeaters, with the line length remaining constant. As discussed in Section 2, it is expected that the throughput will eventually saturate as the number of repeaters continue to increase. This is illustrated by the decreasing throughput / repeaters slope as the graph moves from left to right.

5.4 Conclusion and Future Work

Data collected from this research indicates that a low-power, high throughput global interconnect design can be achieved using high-threshold voltage repeaters and repeater insertion. While not measured in this project, the gains in static power consumption achieved from a high V_t will be reduced as more repeaters are inserted. Future work could investigate this relationship.

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